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ACT–F1M32 High Speed 32 Megabit Boot Block FLASH Multichip Module

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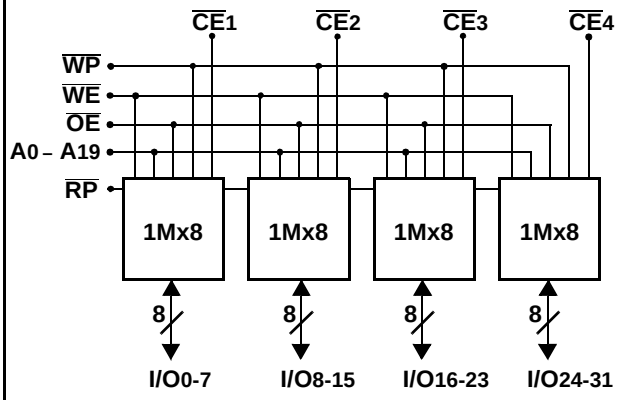
Features

- 4 Low Voltage/Power Intel 1M x 8 FLASH Die in One MCM Package
- Overall Configuration is 1M x 32
- +5V Operation (Standard) or +3.3V (Consult Factory)
- Access Times of 80, 100 and 120 nS (5V Vcc)
- +5V or +12V Programing
- Erase/Program Cycles
  - 100,000 Commercial
  - 10,000 Military and Industrial
- Sector Architecture (Each Die)
  - One 16K Protected Boot Block (*Bottom Boot Block Standard, Top Boot Block Special Order*)
  - Two 8K Parameter Blocks
  - One 96K Main Block
  - Seven 128K Main Blocks
- Single Block Erase (All bits set to 1)
- Hardware Data Protection Feature
- Independent Boot Block Locking
- MIL-PRF-38534 Compliant MCMs Available
- Packaging – Hermetic Ceramic
  - 68 Lead, .94" x .94" x .180" Dual-Cavity Small Outline Gull Wing, Aeroflex code# "F14" *(Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint)*
- Internal Decoupling Capacitors for Low Noise Operation
- Commercial, Industrial and Military Temperature Ranges

Block Diagram – CQFP(F14)

Standard Configuration

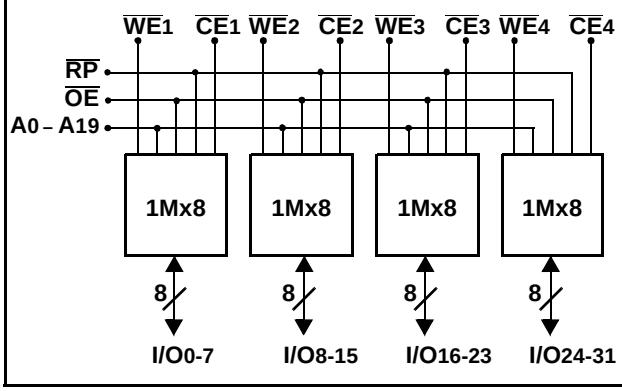


Pin Description

I/O0-31	Data I/O
A0–19	Address Inputs
WE	Write Enables
CE1-4	Chip Enables
OE	Output Enable
WP	Write Protect
RP	Reset/Powerdown
VCC	Power Supply
GND	Ground
NC	Not Connected

Block Diagram – CQFP(F14)

Optional Configuration



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VCC	Power Supply
GND	Ground
NC	Not Connected

General Description

Utilizing Intel's SmartVoltage Boot Block Flash Memory SmartDie™, the ACT–F1M32 is a high speed, 32 megabit CMOS flash multichip module (MCM) designed for full temperature range military, space, or high reliability applications.

The ACT-F1M32 consists of four high-performance Intel X28F800BV 8 Mbit (8,388,608 bit) memory die. Each die contains separately erasable blocks, including a hardware lockable boot block (16,384 bytes), two parameter blocks (8,192 bytes each), and 8 main blocks (one block of 98,304 bytes and seven blocks of 131,072 bytes) This defines the boot block flash family architecture.

The command register is written by bringing $\overline{WE}$ to a logic low level (V_{IL}), while $\overline{CE}$ is low and $\overline{OE}$ is high (V_{IH}). Reading is

General Description, Cont'd,

accomplished by chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) being logically active. Access time grades of 80nS, 100nS and 120nS maximum are standard.

The ACT–F1M32 is packaged in a hermetically sealed co-fired ceramic 68 lead, .94" SQ Ceramic Gull Wing CQFP package. This allows operation in a military environment temperature range of -55°C to +125°C.

The ACT–F1M32 provides program and erase capability at 5V or 12V and allows reads with Vcc at 5V or 3.3V(Not tested). Since many designs read from flash memory a large percentage of the time, read operation using 3.3V can provide great power savings. Consult the factory for 3.3V tested parts. In applications where read performance is critical, faster access times are obtainable with the 5V V_{CC} part detailed herein.

For program and erase operations, 5V Vpp operation eliminates the need for in system voltage converters. The 12V Vpp operation provides reduced (approx 60%) program and erase times where 12V is available in the system. For design simplicity, however, connect Vcc and Vpp to the same 5V ±10% source.

Each block can be independently erased and programmed 100,000 times at commercial temperature or 10,000 times at extended temperature.

The boot block is located at either the bottom (Standard) or the top (Special Order) of the address map in order to accommodate different microprocessor protocols for boot code location. Locking and unlocking of the boot block is controlled by $\overline{WP}$ and/or $\overline{RP}$.

Intel's boot block architecture provides a flexible solution for the different design needs of various applications. The asymmetrically-blocked memory map allows the integration of several memory components into a single flash device. The boot block provides a secure boot PROM; the parameter blocks can emulate EEPROM functionality for parameter store with proper software techniques; and the main blocks provide code and data storage with access times fast enough to execute code in place, decreasing RAM requirements.

For Detail Information regarding the operation of the 28F800BV Memory die, see the Intel datasheet (order number 290539-002).

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Absolute Maximum Ratings

Parameter	Range	Units
Case Operating Temperature Range	-55 to +125	°C
Storage Temperature Range	-65 to +150	°C
Voltage on Any Pin with Respect to GND (except V_{CC}, V_{PP}, A9 and $\overline{RP}$) (1)	-2.0 to +7.0	V
Voltage on Pins A9 or $\overline{RP}$ with Respect to GND (except V_{CC}, V_{PP}, A9 and $\overline{RP}$) (1,2)	-2.0 to +13.5	V
V_{PP} Program Voltage with Respect to GND during Block Erase/ and Word/Byte Write (1,2)	-2.0 to +14.0	V
Vcc Supply Voltage with Respect to Ground (1)	-2.0 to +7.0	V
Output Short Circuit Current (3)	100	mA

Notes:
1. Minimum DC voltage is -0.5V on input/output pins. During Transitions, inputs may undershoot to -2.0V for periods < 20nS. Maximum DC voltage on input/output pins is Vcc + 0.5V, which may overshoot to Vcc + 2.0V for periods < 20nS.
2. Maximum DC voltage on Vpp may overshoot to +14.0V for periods < 20nS. Maximum DC voltage on $\overline{RP}$ or A9 may overshoot to V_{CC} + 0.5V for periods <20nS
3. Output shorted for no more than 1 second. No more than one output shorted at one time.

NOTICE: Stresses above those listed under "Absolute Maximums Rating" may cause permanent damage. These are stress rating only. Operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may effect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	5V Power Supply Voltage (10%)	+4.5	+5.5	V
	3.3V Power Supply Voltage (±0.3V) (Consult Factory)	+3.0	+3.6	V
V_{IH}	Input High Voltage (3.3V & 5V V_{CC})	+2.0	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage (3.3V & 5V V_{CC})	-0.5	+0.8	V
T_A	Operating Temperature (Military)	-55	+125	°C

Capacitance

(f = 1MHz, T_A = 25°C)

Symbol	Parameter	Maximum	Units
C_{AD}	A0 – A19 Capacitance	50	pF
C_{OE}	$\overline{OE}$ Capacitance	50	pF
C_{CE}	$\overline{CE}$ Capacitance	20	pF
C_{RP}	$\overline{RP}$ Capacitance	50	pF
C_{WE}	$\overline{WE}$ Capacitance	60	pF
C_{WP}	$\overline{WP}$ Capacitance	50	pF
$C_{I/O}$	I/O0 – I/O31 Capacitance	20	pF

Capacitance Guaranteed by design, but not tested.

DC Characteristics – CMOS Compatible

(T_A = -55°C to +125°C, V_{CC} = +4.5V to + 5.5V(5V Operation), or +3.0V to +3.6V(3.3V Operation), Unless otherwise specified)

Parameter	Sym	Conditions	+3.3V Vcc (1) Typical		+5.0V Vcc Standard		Units
			Min	Max	Min	Max	
Input Load Current	I_{IL}	V_{CC} = V_{CC}Max., V_{IN} = V_{CC} or GND	-1	+1	-1	+1	µA
Output Leakage Current	I_{LO}	V_{CC} = V_{CC}Max., V_{IN} = V_{CC} or GND	-10	+10	-10	+10	µA
Vcc Standby Current	I_{CCS}	V_{CC} = V_{CC}Max., $\overline{CE}$ = $\overline{RP}$ = $\overline{WP}$ = V_{CC} ± 0.2V		440		600	µA
Vcc Deep Power-Down Current	I_{CCD}	V_{CC} = V_{CC}Max., V_{IN} = V_{CC} or GND, $\overline{RP}$ = GND ± 0.2V		32		32	µA
Vcc Read Current	I_{CCR}	V_{CC} = V_{CC}Max., $\overline{CE}$ = GND, f = 10MHz (5V), 5MHz (3.3V), I_{OUT} = 0 mA, Inputs = GND ± 0.2V or V_{CC} ± 0.2V		120		260	mA
Vcc Write Current	I_{CCW1}	V_{PP} = V_{PPH1} (at 5V), Word Write in Progress (x32)		120		200	mA
	I_{CCW2}	V_{PP} = V_{PPH2} (at 12V), Word Write in Progress (x32)		100		180	mA
Vcc Erase Current	I_{CCE1}	V_{PP} = V_{PPH1} (at 5V),Block Erase in Progress		120		180	mA
	I_{CCE2}	V_{PP} = V_{PPH2} (at 12V),Block Erase in Progress		100		160	mA
Vcc Erase Suspend Current	I_{CCES}	$\overline{CE}$ = V_{IH}, Block Erase Suspend		32		48	mA
V_{PP} Standby Current	I_{PPS}	V_{PP} < V_{PPH2}		60		60	µA

DC Characteristics – CMOS Compatible

(T_A = -55°C to +125°C, V_{CC} = +4.5V to + 5.5V(5V Operation), or +3.0V to +3.6V(3.3V Operation), Unless otherwise specified)

Parameter	Sym	Conditions	+3.3V Vcc (1) Typical		+5.0V Vcc Standard		Units
			Min	Max	Min	Max	
V_{PP} Deep Power Down Current	I_{PPD}	$\overline{RP}$ = GND ± 0.2V		40		40	µA
V_{PP} Read Current	I_{PPR}	$V_{PP} \geq V_{PPH2}$		800		800	µA
V_{PP} Write Current	I_{PPW1}	$V_{PP} = V_{PPH1}$ (at 5V), Word Write in Progress (x32)		120		120	mA
	I_{PPW2}	$V_{PP} = V_{PPH2}$ (at 12V), Word Write in Progress (x32)		100		100	mA
V_{PP} Erase Current	I_{PPE1}	$V_{PP} = V_{PPH1}$ (at 5V), Block Erase in Progress		120		100	mA
	I_{PPE2}	$V_{PP} = V_{PPH2}$ (at 12V), Block Erase in Progress		100		80	mA
V_{PP} Erase Suspend Current	I_{PPES}	$V_{PP} = V_{PPH}$, Block Erase Suspend in Progress		800		800	µA
$\overline{RP}$ Boot Block Unlock Current	I_{RP}	$\overline{RP} = V_{HH}$, V_{PP} = 12V		2		2	mA
Output Low Voltage	V_{OL}	$V_{CC} = V_{CC}$Min., I_{OL} = 5.8 mA (5V), 2 mA (3.3V)		0.45		0.45	V
Output High Voltage	V_{OH1}	$V_{CC} = V_{CC}$Min., I_{OH} = -2.5 mA	0.85 x V_{CC}		0.85 x V_{CC}		V
	V_{OH2}	$V_{CC} = V_{CC}$Min., I_{OH} = -100 µA	V_{CC} - 0.4V		V_{CC} - 0.4V		V
V_{PP} Lock-Out Voltage	V_{PPLK}	Complete Write Protection	0.0	1.5	0.0	1.5	V
V_{PP} (Program/Erase Operations)	V_{PPH1}	V_{PP} = at 5V	4.5	5.5	4.5	5.5	V
V_{PP} (Program/Erase Operations)	V_{PPH2}	V_{PP} = at 12V	11.4	12.6	11.4	12.6	V
V_{CC} Erase/Write Lock Voltage	V_{LKO}	Locked Condition	0	2.0	0	2.0	V
$\overline{RP}$ Unlock Voltage	V_{HH}	Boot Block Write/Erase, V_{PP} = 12V	11.4	12.6	11.4	12.6	V

Notes:
1. Performance at V_{CC} = +4.5V to +5.5V is guaranteed. Performance at V_{CC} = +3.3V is typical (Not tested).

AC Characteristics – Write/Erase/Program Operations – $\overline{WE}$ Controlled

(T_A = -55°C to +125°C, V_{CC} = +4.5V to + 5.5V(5V Operation), or +3.0V to +3.6V(3.3V Operation), Unless otherwise specified)

Parameter	Symbol JEDEC Standard	+3.3V Vcc (2) Typical		+4.5V to +5.5V Vcc						Units
		120nS		80nS		100nS		120nS		
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	120		80		100		120		nS
$\overline{RP}$ High Recovery to $\overline{WE}$ Going Low	t_{PHWL}	1.5		.45		.45		.45		µS
$\overline{CE}$ Setup to $\overline{WE}$ Going Low	t_{ELWL}	0		0		0		0		nS
Boot Block Unlock Setup to $\overline{WE}$ Going High (1)	t_{PHHWH}	200		100		100		100		nS
V_{PP} Setup to $\overline{WE}$ Going High (1)	t_{VPWH}	200		100		100		100		nS
Address Setup to $\overline{WE}$ Going High	t_{AVWH}	90		60		60		60		nS
Data Setup to $\overline{WE}$ Going High	t_{DVWH}	70		60		60		60		nS
$\overline{WE}$ Pulse Width	t_{WLWH}	90		60		60		60		nS
Data Hold Time from $\overline{WE}$ High	t_{WHDX}	0		0		0		0		nS
Address Hold Time from $\overline{WE}$ High	t_{WHAX}	0		0		0		0		nS
$\overline{CE}$ Hold Time from $\overline{WE}$ High	t_{WHEH}	0		0		0		0		nS
$\overline{WE}$ Pulse Width High	t_{WHWL}	30		20		20		20		nS
Duration of Word Write Operation (1) (x32)	t_{WHQV1}	6		6		6		6		µS
Duration of Erase Operation (Boot) (1)	t_{WHQV2}	0.3		0.3		0.3		0.3		Sec
Duration of Erase Operation (Parameter) (1)	t_{WHQV3}	0.3		0.3		0.3		0.3		Sec
Duration of Erase Operation (Main) (1)	t_{WHQV4}	0.6		0.6		0.6		0.6		Sec
V_{PP} Hold from Valid SRD (1)	t_{QVVL}	0		0		0		0		nS
$\overline{RP}$ V_{HH} Hold from Valid SRD (1)	t_{QVPH}	0		0		0		0		nS
Boot Block Lock Delay (1)	t_{PHBR}		200		100		100		100	nS

Notes:
1. Guaranteed by design, not tested.
2. Performance at V_{CC} = +4.5V to +5.5V is guaranteed. Performance at V_{CC} = +3.3V is typical (Not tested).

AC Characteristics – Write/Erase/Program Operations, $\overline{CE}$ Controlled

(T_A = -55°C to +125°C, V_{CC} = +4.5V to + 5.5V(5V Operation), or +3.0V to +3.6V(3.3V Operation), Unless otherwise specified)

Parameter	Symbol JEDEC Standard	+3.3V V_{CC} [2] Typical		+4.5V to +5.5V V_{CC}						Units
		120nS		80nS		100nS		120nS		
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	120		80		100		120		nS
$\overline{RP}$ High Recovery to $\overline{CE}$ Low	t_{PHEL}	1.5		.45		.45		.45		µS
$\overline{WE}$ Setup to $\overline{CE}$ Going Low	t_{WLEL}	0		0		0		0		nS
Boot Block Unlock Setup to $\overline{CE}$ Going High [1]	t_{PHHEH}	200		100		100		100		nS
V_{PP} Setup to $\overline{CE}$ Going High [1]	t_{VPEH}	200		100		100		100		nS
Address Setup to $\overline{CE}$ Going High	t_{AVEH}	90		60		60		60		nS
Data Setup to $\overline{CE}$ Going High	t_{DVEH}	70		60		60		60		nS
$\overline{CE}$ Pulse Width	t_{ELEH}	90		60		60		60		nS
Data Hold Time from $\overline{CE}$ High	t_{EHDX}	0		0		0		0		nS
Address Hold Time from $\overline{CE}$ High	t_{EHAX}	0		0		0		0		nS
$\overline{WE}$ Hold Time from $\overline{CE}$ High	t_{EHWH}	0		0		0		0		nS
$\overline{CE}$ Pulse Width High	t_{EHEL}	20		20		20		20		nS
Duration of Word Write Operation [1] (x32)	t_{EHQV1}	6		6		6		6		µS
Duration of Erase Operation (Boot) [1]	t_{EHQV2}	0.3		0.3		0.3		0.3		Sec
Duration of Erase Operation (Parameter) [1]	t_{EHQV3}	0.3		0.3		0.3		0.3		Sec
Duration of Erase Operation (Main) [1]	t_{EHQV4}	0.6		0.6		0.6		0.6		Sec
V_{PP} Hold from Valid SRD [1]	t_{QVVL}	0		0		0		0		nS
$\overline{RP}$ V_{HH} Hold from Valid SRD [1]	t_{QVPH}	0		0		0		0		nS
Boot Block Lock Delay [1]	t_{PHBR}		200		100		100		100	nS

NOTES:
1. Sampled, but not 100% tested.
2. Performance at V_{CC} = +4.5V to +5.5V is guaranteed. Performance at V_{CC} = +3.3V is typical (Not Tested).

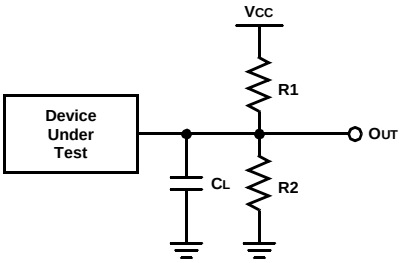
AC Characteristics – Read Only Operations

(T_A = -55°C to +125°C, V_{CC} = +4.5V to + 5.5V(5V Operation), or +3.0V to +3.6V(3.3V Operation), Unless otherwise specified)

Parameter	Symbol JEDEC Standard	+3.3V V_{CC} [2] Typical		+4.5V to +5.5V V_{CC}						Units
		120nS		80nS		100nS		120nS		
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	120		80		100		120		nS
Address to Output Delay	t_{AVQV}		120		80		100		120	nS
$\overline{CE}$ to Output Delay	t_{ELQV}		120		80		100		120	nS
$\overline{RP}$ to Output Delay	t_{PHQV}		1.5		.45		.45		.45	µS
$\overline{OE}$ to Output Delay	t_{GLQV}		65		40		40		40	nS
$\overline{CE}$ to Output in Low Z [1]	t_{ELQX}	0		0		0		0		nS
$\overline{CE}$ to Output in High Z [1]	t_{EHQZ}		55		30		30		30	nS
$\overline{OE}$ to Output in Low Z [1]	t_{GLQX}	0		0		0		0		nS
$\overline{OE}$ to Output in High Z [1]	t_{GHQZ}		45		30		30		30	nS
Output Hold from Address, $\overline{CE}$, or $\overline{OE}$ Change, Whichever Occurs First [1]	t_{OH}	0		0		0		0		nS

Notes:
1. Guaranteed by design, but not tested.
2. Performance at V_{CC} = +4.5V to +5.5V is guaranteed. Performance at V_{CC} = +3.3V is typical (Not Tested).

AC Test Circuit



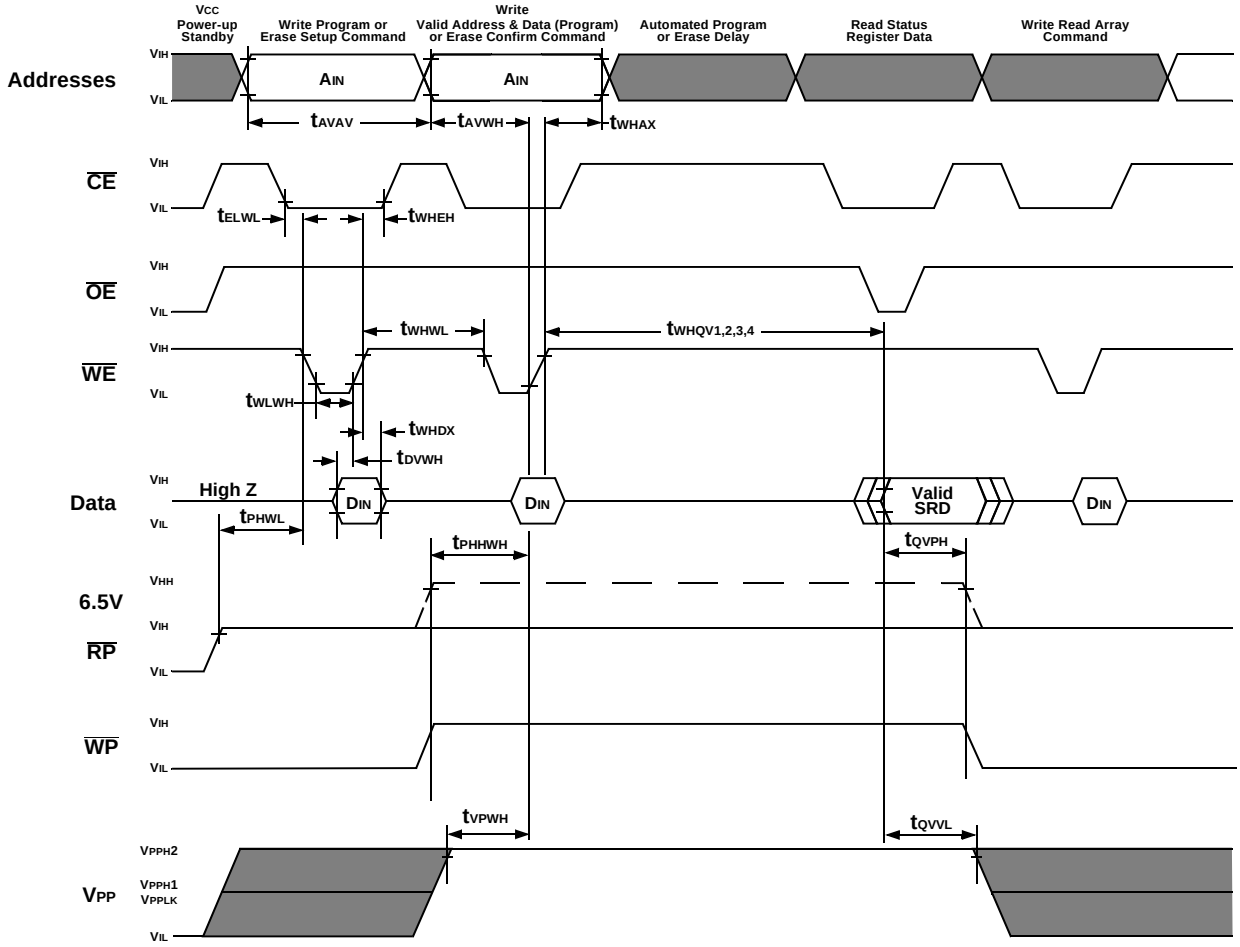
Test Configuration Component Values

Test Configuration	C_L (pF)	R1 (Ω)	R2 (Ω)
3.3V Standard Test	50	990	770
5V Standard Test	50	580	390

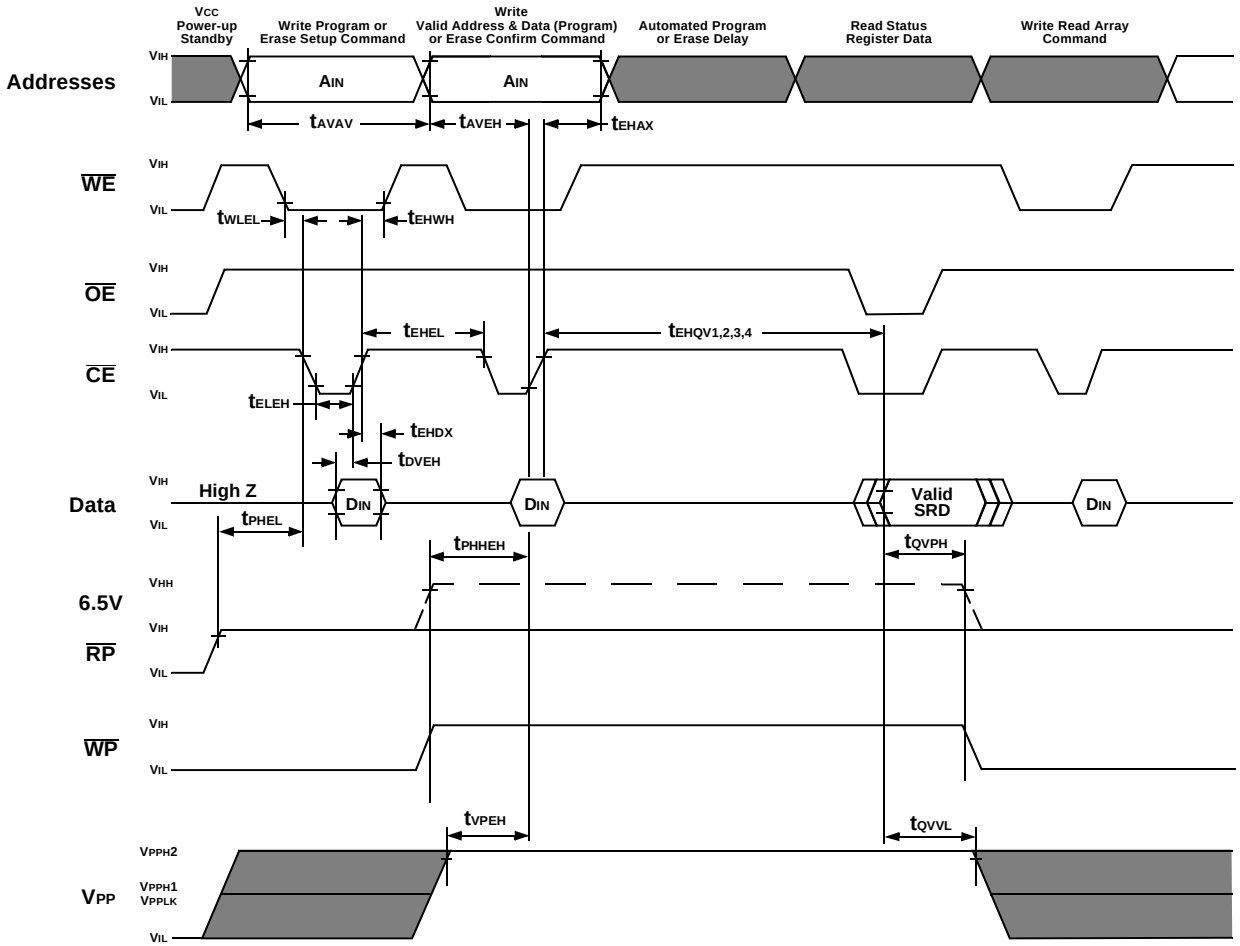
NOTES:
C_L includes jig capacitance.

Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	nS
Input and Output Timing Reference Level	1.5	V

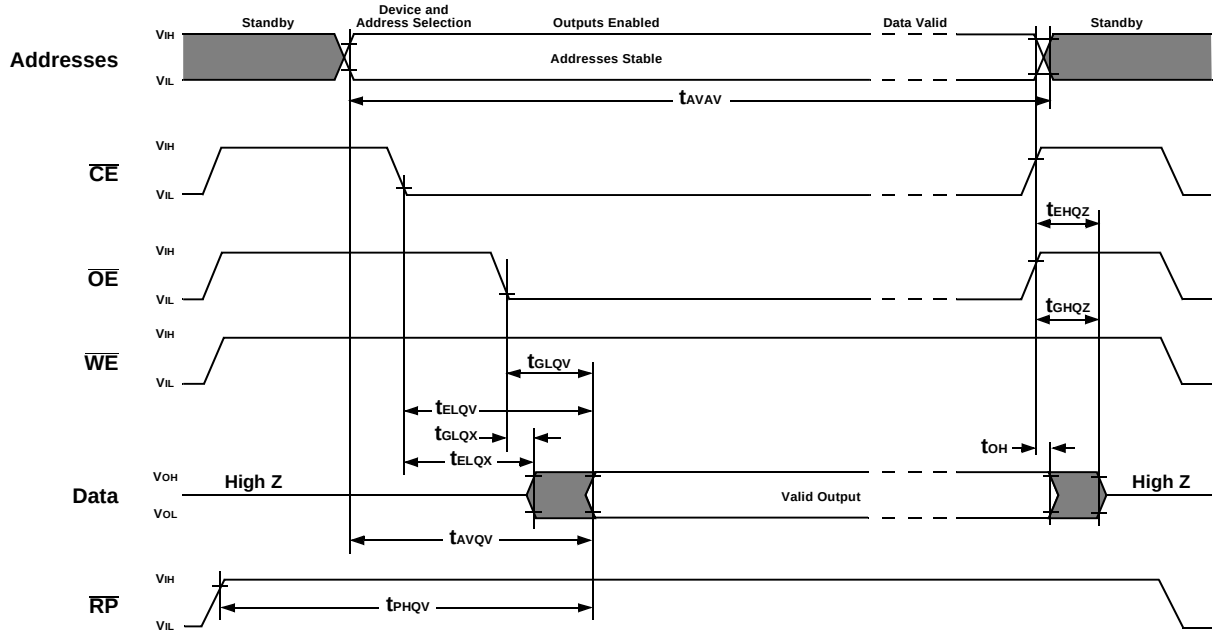
AC Waveforms for Write and Erase Operations, $\overline{WE}$ Controlled



AC Waveforms for Write and Erase Operations, $\overline{CE}$ Controlled



AC Waveform For Read Operations

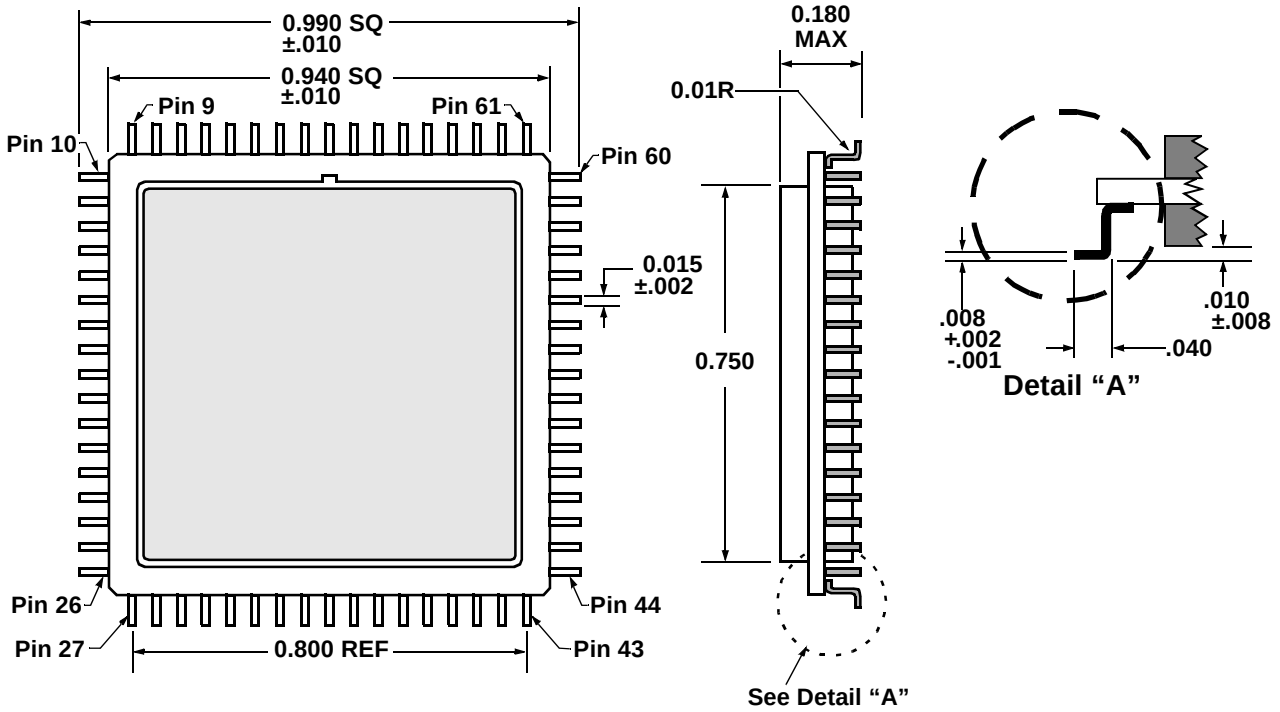


Pin Numbers & Functions

68 Pins — Dual-Cavity CQFP *(Standard Configuration)*							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CE}_3$	19	I/O_8	36	$\overline{CE}_2$	53	I/O_{23}
3	A_5	20	I/O_9	37	A_{17}	54	I/O_{22}
4	A_4	21	I/O_{10}	38	$\overline{WP}$	55	I/O_{21}
5	A_3	22	I/O_{11}	39	NC	56	I/O_{20}
6	A_2	23	I/O_{12}	40	NC	57	I/O_{19}
7	A_1	24	I/O_{13}	41	A_{18}	58	I/O_{18}
8	A_0	25	I/O_{14}	42	A_{19}	59	I/O_{17}
9	$\overline{RP}$	26	I/O_{15}	43	V_{PP}	60	I/O_{16}
10	I/O_0	27	V_{CC}	44	I/O_{31}	61	V_{CC}
11	I/O_1	28	A_{11}	45	I/O_{30}	62	A_{10}
12	I/O_2	29	A_{12}	46	I/O_{29}	63	A_9
13	I/O_3	30	A_{13}	47	I/O_{28}	64	A_8
14	I/O_4	31	A_{14}	48	I/O_{27}	65	A_7
15	I/O_5	32	A_{15}	49	I/O_{26}	66	A_6
16	I/O_6	33	A_{16}	50	I/O_{25}	67	$\overline{WE}$
17	I/O_7	34	$\overline{CE}_1$	51	I/O_{24}	68	$\overline{CE}_4$

Consult Factory for Special order *(Optional Configuration)*: Pin 38 - $\overline{WE}_2$, Pin 39 - $\overline{WE}_3$, Pin 40 - $\overline{WE}_4$ and Pin 67 - $\overline{WE}_1$

"F14" — CQFP Dual-Cavity Flat Package



All dimensions in inches

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Ordering Information

Model Number	Screening	Speed	Package
ACT–F1M32B–080F14C	Commercial (0°C to +70°C)	80 nS	CQFP
ACT–F1M32B–100F14C	Commercial (0°C to +70°C)	100 nS	CQFP
ACT–F1M32B–120F14C	Commercial (0°C to +70°C)	120 nS	CQFP
ACT–F1M32B–080F14I	Industrial (-40°C to +85°C)	80 nS	CQFP
ACT–F1M32B–100F14I	Industrial (-40°C to +85°C)	100 nS	CQFP
ACT–F1M32B–120F14I	Industrial (-40°C to +85°C)	120 nS	CQFP
ACT–F1M32B–080F14M	Military (-55°C to +125°C)	80 nS	CQFP
ACT–F1M32B–100F14M	Military (-55°C to +125°C)	100 nS	CQFP
ACT–F1M32B–120F14M	Military (-55°C to +125°C)	120 nS	CQFP
ACT–F1M32B–080F14Q	DESC Drawing Pending MIL-PRF-38534 Compliant	80 nS	CQFP
ACT–F1M32B–100F14Q	DESC Drawing Pending MIL-PRF-38534 Compliant	100 nS	CQFP
ACT–F1M32B–120F14Q	DESC Drawing Pending MIL-PRF-38534 Compliant	120 nS	CQFP

Part Number Breakdown

ACT– F 1M 32 B– 080 F14 M

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Memory Type

S = SRAM
F = FLASH EEPROM
E = EEPROM
D = Dynamic RAM

Memory Depth, Locations

Memory Width, Bits

Pinout Options

B = Bottom Boot Block (Standard),
T= Top Boot Block (Special Order)

Memory Speed, ns (+5V Vcc)

Screening

C = Commercial Temp, 0°C to +70°C
I = Industrial Temp, -40°C to +85°C
T = Military Temp, -55°C to +125°C
M = Military Temp, -55°C to +125°C, Screened *
Q = MIL-PRF-38534 Compliant/SMD if applicable

Package Type & Size

Surface Mount Packages
F14 = .94" SQ 68 Lead\Dual-Cavity CQFP

* **Screened to the individual test methods of MIL-STD-883**

Specifications subject to change without notice

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